

APPLICATION FOR UNITED STATES PATENT

FOR

LOW-K INTERLAYER DIELECTRIC WAFER GRINDING

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TECHNICAL FIELD & BACKGROUND

The present disclosure is related to the field of semiconductor device manufacturing and packaging. More specifically but not exclusively, the present disclosure is related to grinding of semiconductor wafers having low-K interlayer dielectric (ILD) layers.

The desire for thinner wafers and enhanced performance of integrated circuits has led to the integration of low-K (low-dielectric constant) interlayer dielectrics into semiconductor devices. Low-K dielectrics have lower dielectric constant values than materials such as silicon dioxide ($K \sim 4$) and thus are able to reduce the capacitance between metal interconnects on a chip or integrated circuit die, allowing faster and smaller integrated circuits. The use of low-K dielectrics as insulators in semiconductor wafers, however, creates difficulties during wafer packaging assembly operations. For example, grinding of low-K wafers using conventional wafer grinding processes has proven impractical because low-K dielectrics display poor adhesion and fragility. Additionally, wafer sawing may be difficult because cracks often propagate from the dicing saw through the wafer and into the integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be described by way of exemplary
5 embodiments, but not limitations, illustrated in the accompanying drawings in
which like references denote similar elements, and in which:

Figures 1a and 1b illustrate two profiles of conventional grinding chucks
used in semiconductor wafer grinding;

Figure 2 illustrates a top-down and enlarged partial view of a
10 semiconductor wafer having a low-K interlayer dielectric (ILD) layer;

Figure 3 illustrates a grinding method for a semiconductor wafer having a
low-K ILD layer, in accordance with one embodiment; and

Figure 4 illustrates a grinding method for a semiconductor wafer having a
low-K ILD layer, in accordance with another embodiment.

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DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

Embodiments of the present invention include, but are not limited to, methods of low-K interlayer dielectric wafer grinding.

5 Various aspects of the illustrative embodiments will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that embodiments of the present invention may be practiced with only some of the described aspects. For purposes of explanation, specific numbers,
10 materials and configurations are set forth in order to provide a thorough understanding of the illustrative embodiments. However, it will be apparent to one skilled in the art that embodiments of the present invention may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative embodiments.

15 Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present invention, however, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

20 The phrase "in one embodiment" is used repeatedly. The phrase generally does not refer to the same embodiment, however, it may. The terms "comprising", "having" and "including" are synonymous, unless the context dictates otherwise.

 Embodiments of a method for grinding a semiconductor wafer having a
25 low-K interlayer dielectric (ILD) layer are discussed below. For simplicity and clarity of explanation, various embodiments of the invention are shown in the

figures according to various views. It is to be appreciated that such views are merely illustrative and are not necessarily drawn to scale or to the exact shape. Furthermore, it is to be appreciated that the actual devices utilizing principles of the invention may vary in shape, size, configuration, contour, and the like, other
5 than what is shown in the figures, due to different manufacturing processes, equipment, design tolerances, or other practical considerations that result in variations from one semiconductor device to another.

Figures 1a and 1b illustrate two example profiles of conventional grinding chucks used in thinning or grinding a backside (i.e., lower surface or non-active
10 side) of a semiconductor wafer. In grinding, the semiconductor wafer may be held face-down on a vacuum chuck as a series of progressively finer grinding wheels or chucks are moved over the backside of the semiconductor wafer while it is rotated on a turntable. Rather than having a flat grinding surface, such grinding chucks usually have either a convex shape as shown in **Figure 1a** or a
15 concave shape as shown in **Figure 1b**. Resultantly, grinding stresses and forces may tend to concentrate into highly stressed areas at or near the center of the semiconductor wafer, rather than being distributed evenly across the wafer (as it would, for example, if the grinding chuck were flat). Semiconductor wafers having ILD layers with higher dielectric constants (for example, as discussed
20 previously, silicon dioxide where $K \sim 4$) are generally able to withstand such grinding stresses, however, wafers including one or more low-K ILD layers (or simply, "low-K ILD wafers") are weaker and grinding may cause cracks to propagate throughout the semiconductor wafer. For these reasons, low-K ILD wafers may not usually be grinded using mechanical grinding processes similar
25 to those described above.

Similarly, low-K ILD wafers may not be singulated using typical sawing processes for semiconductor wafers because of the fragility and poor adhesion of low-K ILD layers. Thus, laser scribing before sawing may often be required to separate or singulate low-K ILD wafers. A prior art method of singulation of low-K ILD wafers uses lasers to scribe through a low-K ILD layer on the wafer to prevent cracks from propagating from a dicing saw through the wafer and into the integrated circuit. To illustrate, **Figure 2** is a top-down and enlarged partial view of a low-K ILD wafer **202**. In **Figure 2**, a laser may be used to scribe or form two trenches or laser scribe lines **206** along either side of streets separating a plurality of adjacent integrated circuit devices or dice **204** on a front side **205** of wafer **202**. The laser may scribe through the low-K ILD layer and stop at the silicon of wafer **202**. A saw may then dice or cut along approximately a center of the streets to a width of a saw cut as illustrated by a plurality of saw kerfs **208**. In doing so, the saw dices or cuts through both the low-K ILD layer and silicon, to singulate wafer **202** into individual dice or a plurality of dice. Note that cracks created by the saw may be stopped on either side of saw kerf **208** as they reach laser scribe lines **206**, as illustrated by reference lines **212**.

Figure 3 illustrates a grinding method for wafer **202** in accordance with one embodiment. In **Figure 3**, for the embodiment, a backside **309** of wafer **202** may be mounted with an adhesive or wafer mounting tape **312(a)**. In the embodiment, laser **303** forms laser scribe lines **206** along sides of streets on front side **205** of wafer **202** to form trenches in the low-K ILD layer as described in **Fig. 2** above. Further, for the embodiment, a saw may then dice or cut wafer **202** along the formed trenches to a width similar to saw kerfs **208** (see **Fig. 2**) to singulate wafer **202** into a plurality of individual dice at **314**. Note that for the

embodiment, the dice may be singulated but are retained on mounting tape **312(a)**.

Note that in various embodiments, other laser scribing and sawing methods may be used to partially dice or dice wafer **202**. For example, although
5 not pictured, laser **303** may form trenches in the low-K ILD layer along streets of wafer **202** that may be wider than the saw kerfs **208** in another embodiment.

Next, a backgrind tape or grinding protection tape **302** may be attached to wafer **202** to protect dice on front side **205** during grinding in the embodiment. In various embodiments, grinding protection tape **302** may be any type of protective
10 layer or protective coating to protect front side **205** of wafer **202** during grinding.

Next, grinding protection tape **302** and mounting tape **312(a)** may be cut at **316** to define a perimeter of wafer **202** or approximate a shape of wafer **202**. Further, for the embodiment, mounting tape **312(a)** may be removed from backside **309** of wafer **202** to prepare for grinding. Wafer **202** may then be
15 mounted face-down on a vacuum chuck **306** so that grinding chuck **320** may grind wafer **202** to a desired wafer thickness. Note that in the embodiment, cracks created in a low-K ILD layer of wafer **202** during grinding or sawing may not propagate because wafer **202** has already been singulated into individual dice.

20 Finally, in the embodiment, backside **309** of thinned and singulated wafer **202** may be mounted with mounting tape **312(b)** onto a wafer frame **325**. In the embodiment, grinding protection tape **302** may then be removed or de-taped from upper surface **205** of wafer **202**.

Figure 4 illustrates a simplified embodiment of the grinding method of
25 wafer **202** illustrated in **Figure 3**. Note that for the embodiment of **Figure 4**, wafer **202** need not be mounted prior to laser scribing. For example, in one

embodiment, wafer **202** may be held on a vacuum chuck during laser scribing (not shown). Thus, mounting tape **312(a)** need not be later removed from wafer **202** nor cut to define a perimeter of wafer **202** as described in **Figure 3**. In **Figure 4**, laser **303** may form laser scribe lines **206** along either side of streets on front side **205** of wafer **202** to form trenches in the low-K ILD layer in the embodiment. Wafer **202** may then be singulated at **314** by a saw into a plurality of individual dice. Note that in another embodiment, wafer **202** may be diced to a thickness deeper than a final desired wafer thickness but not completely through the wafer. Next, for the embodiment, grinding protection tape **302** may be attached to front side **205** to protect front side **205** of wafer **202** during grinding.

For the embodiment, wafer **202** may then be mounted face-down on vacuum chuck **306** to be grinded by grinding chuck **320** to a desired wafer thickness. Note that in the embodiment, cracks created in a low-K ILD layer of wafer **202** during grinding may not propagate because stresses may be distributed more evenly across wafer **202** as wafer **202** has already been singulated into separate dice.

Finally, for the embodiment, backside **309** of grinded and singulated wafer **202** may be mounted with mounting tape **312**. In the embodiment, wafer **202** may be mounted onto a wafer frame **325**. Grinding protection tape **302** may then be removed or de-taped from front side **205** of wafer **202**.

Thus, it can be seen from the above descriptions, one or more novel methods for low-K ILD wafer grinding have been described. While the present invention has been described in terms of the foregoing embodiments, those skilled in the art will recognize that the invention is not limited to the embodiments described. Embodiments of the present invention can be practiced

with modification and alteration within the spirit and scope of the appended claims.

Thus, the description is to be regarded as illustrative instead of restrictive on the present invention.